REMARKS

Claims 21 and 23-40 are pending in the application; of these, Claim 21 is the only independent claim. It is gratefully acknowledged that Claims 35-37 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. The Examiner rejected Claims 21, 23-27, 29-30, 33-34 and 38-40 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,510,630 (Agarwal) in view of U.S. Patent No. 6,229,161 B1 (Nemati) and further in view of U.S. Patent No. 5,821,591 (Krautschneider). Claim 28 was rejected under 35 U.S.C. §103(a) as being unpatentable over Agarwal, Nemati and Krautschneider and further in view of U.S. Patent No. 6,154,477 (Weidenheimer). Claims 31 and 32 were rejected under 35 U.S.C. §103(a) as being unpatentable over Agarwal, Nemati and Krautschneider and further in view of U.S. Patent No.6,391,720 B1 (Sneelal).

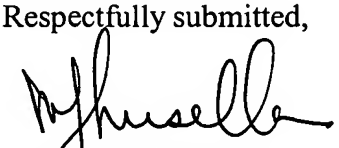
Regarding the Examiner's rejection of independent Claim 21, during a telephonic interview between Applicants' representation, Michael J. Musella, Esq. and the Examiner on June 8, 2005, the Examiner recommended that Claim 21 be further distinguished by including a limitation which defined the current flow in the vertical devices as a vertical current flow. Accordingly, Claim 21 has been amended to include such a limitation. Agarwal discloses a non-volatile random-access memory (NVRAM) that uses a simple, single-transistor DRAM cell configuration. Nemati discloses a capacitively coupled NDR device which can be used to implement a variety of semiconductor circuits,

including high-density SRAM cells and power thyristor structures. Krautschneider discloses a memory cell configuration which includes first memory cells with planar MOS transistors and second memory cells with vertical MOS transistors. The planar MOS transistors are disposed on the bottom and on the crown of parallel strip-like trenches and the vertical MOS transistors are disposed on the side walls of the trenches. Moreover, Krautschneider discloses **the vertical MOS transistors** are realized in the side walls of the trenches 5 and **require no area parallel to the main area** 2 as recited at column 8, lines 60-62. In contrast, Claim 21, as amended, includes the limitation "fabricating each of the plurality of T-RAM memory cells over the at least one SiC layer, wherein each of the plurality of T-RAM memory cells includes a first and a second vertical device, said first and second vertical device being approximately the same height and current flow through the first and second vertical device is predominately in a vertical direction," which is neither taught nor suggested by Agarwal, Nemati or Krautschneider, or any combination thereof. Accordingly, it is respectfully requested that the rejection under 35 U.S.C. §103(a) of Claim 21 be withdrawn.

Independent Claim 21 is believed to be in condition for allowance. Without conceding the patentability per se of dependent Claims 23-34 and 38-40, these are likewise believed to be allowable by virtue of their dependence on Claim 21. Accordingly, reconsideration and withdrawal of the rejections of dependent Claims 23-34 and 38-40 is respectfully requested.

Accordingly, all of the claims pending in the Application, namely, Claims 21 and 23-40, are believed to be in condition for allowance. Should the Examiner believe that a telephone conference or personal interview would facilitate resolution of any remaining matters, the Examiner may contact Applicants' attorney at the number given below.

Respectfully submitted,



Michael M. Musella
Reg. No. 39,310
Attorney for Applicant

DILWORTH & BARRESE, LLP
333 Earle Ovington Blvd.
Uniondale, New York 11553
Tel: (516) 228-8484
Fax: (516) 228-8516

MJM/VAG/ml